LOW VOLTAGE, LOW POWER CMOS OPERATIONAL AMPLIFIER INPUT STAGE

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I.ABSTRACT

The lowering of the power supply and voltage has an enormous impact on the signal to noise ratio (SNR) of analog circuits.
The SNR decreases because of the lower allowable signal voltages and also because of higher noise voltages due to low supply currents. To maximise SNR, we have to make the signal as large as possible ideally from rail to rail. Nowedays trend howards low voltage and low power design are mainly driven by the technological limitations of high performances VLSI systems and the increasing demands for long life equipment.

It is well known that rail-to-rail mode operational amplifier with a high common mode rejection ratio are in growing interest. In this work, we are interested on a particular structure of a CMOS input operational amplifiers stages, used very frequentely in analog circuits, for instrumentation applications in very large scale integration (VLSI). Our study relates to a particular differential input stage which functions in rail-to-rail mode(from the positive bias voltage V_{DD} to the negative one V_{SS})
The principal performances aimed for the input stage are a common mode gain as low as possible, a differential gain and a band-width rather high and as possible the most constant on all the common mode range. Finally, we can affirm that the predictions under our consideration at the beginning were confirmed by electric simulation.

II-Introduction

In order to maximise the signal to noise ratio in low voltage design , we must make signals as large as possible, ideally from rail-to-rail., so the amplifier input stage should be able to deal with common-mode input voltage from Raail-to-Rail. This imposes special demands on the common mode input range and the output voltage range amplifiers.
The main purpose of an input stage is to amplify differential signals and reject the common mode input range. Other important specifications of the input stage are the input referred noise, offset, and the common mode rejection ratio.
Our work consists of study an input stage with a common mode input range which extends from rail-to-rail from Vss to $V_{DD.}$ It is then centered on $(V_{ss}+V_{DD})/2$. The principal perfcormances aimings by the stage are its differential gain and a band-width which are as high as possible, and a most constant common mode range with, moreover, a low common mode gain.

II.Conception of the Rail-to-Rail input stage

In order to achieve this Rail-to-Rail input stage , an n-channel (NMOS) and a p-channel (PMOS) input pair are placed in parallel.

A) Simple NMOS and PMOS input stages

So in order to carry out the Rail-to-Rail input stage we will base ourselves on two simple differential stages, which are the most communly used input stages in a single differential pair. This can typically composed of n-channel or p-channel pair , as shown in figure1.

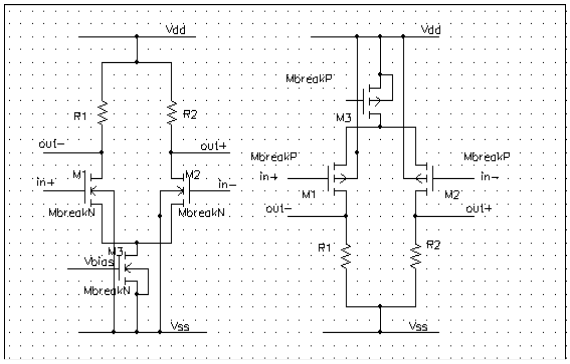

Fig.1. Simple NMOS and PMOS differential stages

resistances play the role of load for the differential pair and the transistor M3 forms the current source.
The working of differential stages depends on the bias voltage of transistors witch depends itself on input voltages and in particular on the common mode voltage.
For the n-channel pair, the common mode input voltage range is given by:

$$V_{SS}+V_{gsn}+V_{dsat}<V_{common}<V_{DD} \quad (1)$$

For the p-channel input pair, the common mode input voltage is given by:

$$V_{SS}<V_{common}<V_{dd}-V_{dsat}-V_{sgp} \quad (2)$$

where:
V_{common} is the common mode input voltage
V_{gsn} the gate-source voltage of the n-channel input transistor
V_{sgp} the source- gate voltage of the input transistor
V_{dsat} the voltage across the drain and source of M3, it is a voltage which is necessary to ensure that M3 is operates as a current source.
V_{DD} the positive supply voltage
V_{SS} the negative voltage supply.

B) Study of input dynamic range of a simple NMOS differential stage

For this study we propose to represent the evolution of drain and source potentials of the input transistors M1 and M2, M3 static current due to the variation of the input common voltage, according to the common mode input voltage for stage NMOS with resistive loads.
When the ccmmon mode voltage varies from Vss to Vdd, we can visualize 4 functioning zones [1].
First we assume that Vthreshold (M1)= Vthreshold (M2)= Vth.

$$*V_{th}(M_1)<V_{MC}<V_{ss}+V_{th}(M1) \quad (3)$$

M1 and M2 are blocked , there is no currents in the differential stage.

$V_{drain}(M1)=V_{DD}$ and $V_{source}(M1)=V_{SS}$, then the current is useless, the differential gain is also equal to 0.

$$*V_{SS}+V_{th}(M_1)<V_{MC}<V_{ss}+V_{th}(M1)+V_{DS}(M3) \quad (4)$$

M3 operate in ohmic region, the continuous currents increase with VMC, V_{GS}(M1)= V_{GS}(M2) increase with the drain current and the drain voltage decreases. The transconductance gm is not constant because the current varies.

$$*V_{SS}+V_{TH}(M1)+V_{DSAT}(M3)<V_{MC}<V_{DD}-V_{DSAT}(M1) \quad -RI_D+V_{GSO} \quad (5)$$

In order that M1, M2 and M3 operate in saturated rgion it is necessary that

$$V_{MC}>V_{SS}+V_{TH}(M1)+V_{DSAT}(M3). \quad (6)$$

The currents in transistors are constant and equal to Icste = I, and VGS(M1)=VGS(M2)=V_{GSO}. Vsource follows the variations of $V_{MC,}$ and Vdrain(M1) = Vdrain(M2)=V_{DD}-RI. In saturation region zone I, VGS, and the transconductance gm are constant.

$$*V_{DD}-(V_{DSAT}(M1)+RI_{cste})<V_{MC}<V_{DD}-V_{GSO}(M1)) \quad (7)$$

When V_{MC} approchs V_{DD}, the transistors currents remain constant, the voltage V_{DS}(M1) = V_{DS}(M2) become lower to V_{DSAT}, M1 and M2 enter in ohmic zone. V_{DS} decrease, and V_{GS} increase.
This s zone exists only if

$$V_{GSO}(M1)<V_{DSAT}(M1)+RI \quad (8)$$

III. Simulation results:

In order to highlight quoted explanations above, we simulate with **WINSPICE** the electric diagram of figure 1 for an input common mode voltage varying from-2.5v to 2.5v, with vss=-2.5v and V_{DD}=2.5v.

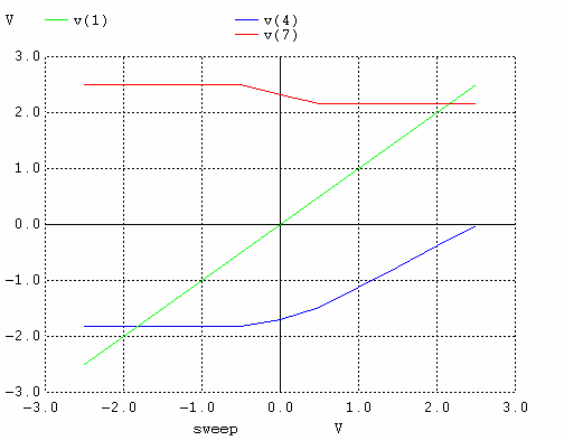

Fig. 2:drain v(7), source(4), and gate(1) voltage of the transistor M1 according to the common mode input voltage

We can check that M3 works as a current source (figure.3.), for this we represent V_{DS} and $V_{DSAT}=V_{GS} - V_{TH}$, we observe that $V_{DS} > V_{DSAT}$, We can affirm that M3 is in saturated region.

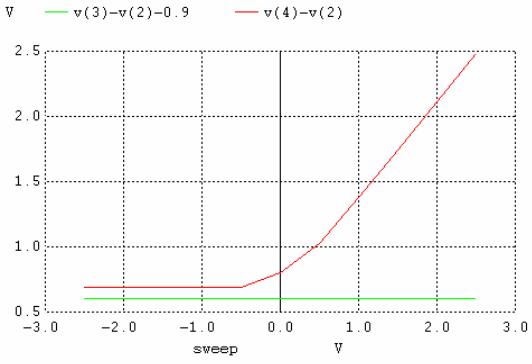

Fig. 3: V_{DS} and V_{DSAT} of M3 according to the common mode input voltage.

V(3) is the gate voltage, v(2) the source voltage, v(4) the drain voltage and V_{TH}(M1)=0.9v.

The simulation results are in agreement with the results of the qualitative study which preceded. The drain current increases with V_{MC}. In order to decrease the loss of gain we can lower resistance values, or to exploit the Vdsat tension by reducing the ratio W/L of the input transistors .

C) NMOS differential stage with transistors loads

For obstruction reasons , it is in habit in CMOS technology to replace the resistive loads by transistors assembled in diode. Within the framework of our study, let us consider a NMOS differantial stage where resistances are replaced by transistors PMOS M5 and M6 as illustrated on the figure.4., these transistors are always saturated.

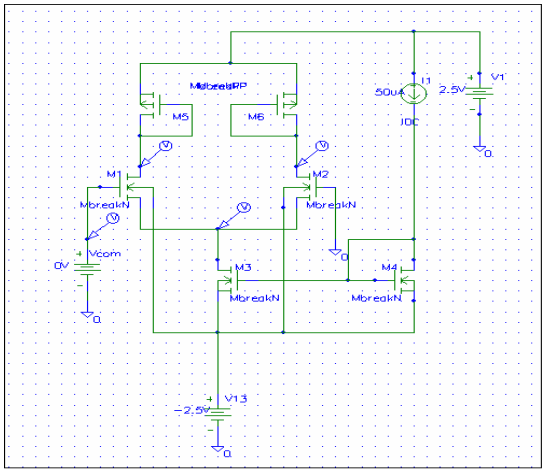

Fig. 4:NMOS differential stage with transistors loads

IV. Simulation results:

Let us represent in the same manner the evolution of Vdrain v(3), Vsource v(6) and Vgate v(7) according to the common mode input voltage.

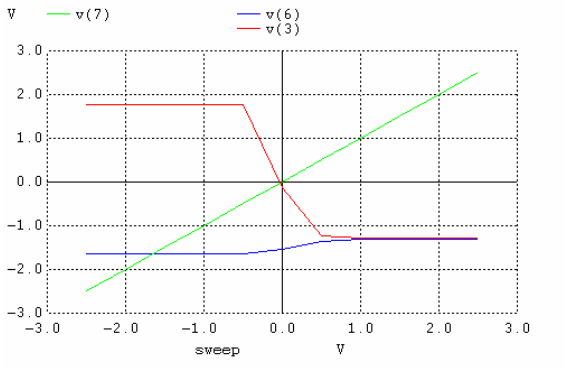

Fig. 5:drain , source, and gate voltage of the transistor M1 according to the common mode input voltage.

Here we can remarque that the output voltage Vdrain represents by V(3) is not equal to V_{DD} which is equal to 2.5v when $Vss<V_{MC}<V_{TH}$(M1) that is explained by pointing out the characteristic of transistor PMOS assembled in diode, of which resistance varies with its operation point , the leakage currents generent a fall of potential at the transistors boundaries assembled in diode whose resistance can reach several giga-ohms .
The AC and the transient simulation are represented in figure.6. and 7 for out+ and out-.

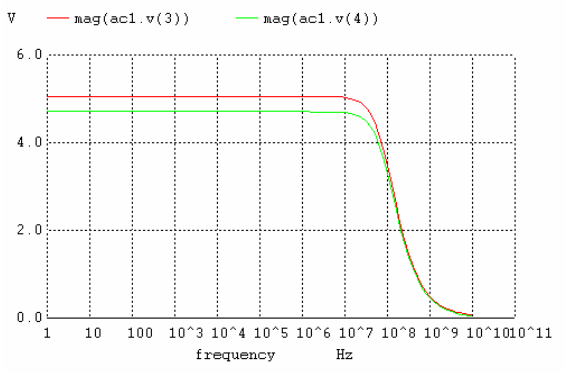

Fig. 6:AC analysis

On the figure.6. is represented the amplitude of the differential gain according to the frequency of the input signal .
On this figure, it appears that the differential low frequency gain remains appreciably constant then falls beyond a certain frequency.

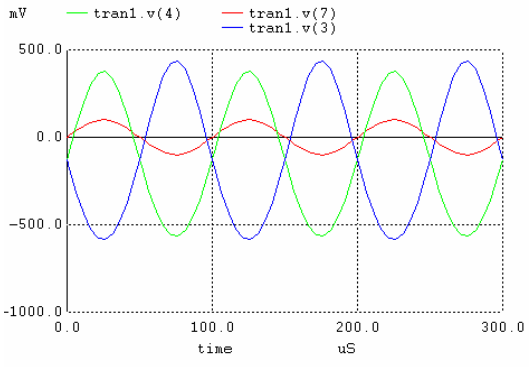

Fig.7.: transient analysis

On figure.7., we can appreciate the amplification of the
nput signal V(7).here we consider out+ and out-

D) Rail to Rail input stage

The considered input stage of the amplifier we intended to use has to have a common mode input range which extends from rail to rail. In order to achieve this, an n-channel and p-channel input pair can be placed in parallel, as is shown in figure.8.

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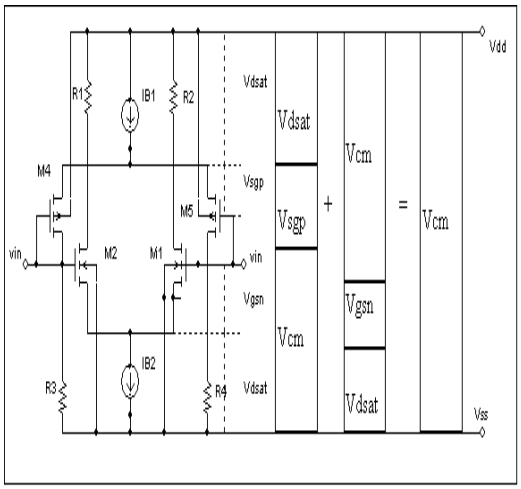

Fig.8.: Common mode input range of a rail-to rail input stage

The n-channel input pair M1-M2 is able to reach the positive supply rail while the p-channel one M4-M5, can sense common mode voltages around the negative supply rail.
In order to ensure a full rail-to rail common mode input voltage range, the supply voltage of the rail to rail input stage requires a supply voltage of at least:

$$V_{\text{sup,min}} = V_{sgp} + V_{gsn} + 2V_{dsat} \qquad (9)$$

If the supply voltage is above the minimum supply voltage, the common mode input voltage range can be devided into the following three parts:

- Low common input mode input voltages: only p-channel input pair operates

- Intermediate common mode input voltages, both of the n-channel an p-channel input pair operate.
- High common mode input voltage, only the n-channel input pair operate.

In order to highlight quoted explanations above, we simulate with **WINSPICE** the electric diagram of the rail-to-rail input stage given in figure.9. for an input common mode voltage varying from-2.5v to 2.5v, with vss=-2.5v and V_{DD}=2.5v., where current source I_{B1} and I_{B2} are replaced by transistors M5, M6 which form current source, the resistive loads R1, R2 of NMOS differential stage are remplaced by PMOS transistors M9, M10 assembled in diode., the PMOS differential pair is loaded with current mirrors instead of resistors R3, R4.

In this electric diagram, we can observe that:

- M3, M4, M6, M7, M8 form PMOS differential stage.
- M1, M2,M5, M10, M9 form NMOS differential stage.
- M8, M11, M12, M7 form current mirrors.

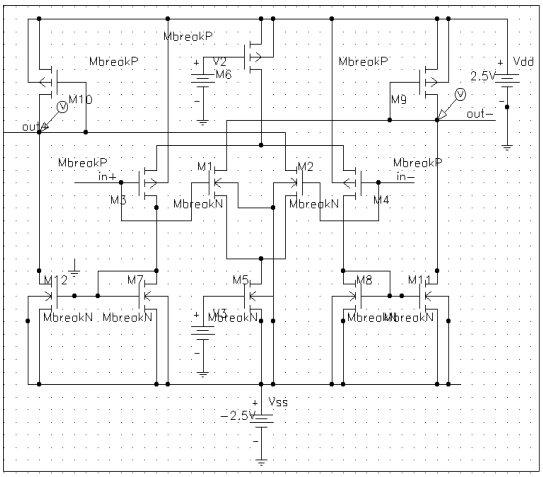

Fig.9.: electric diagram of a Rail-to-Rail differential stage in CMOS technology.

V. Simulation results:

The simulation results we obtain are illustrated by the graphs of the figures below:

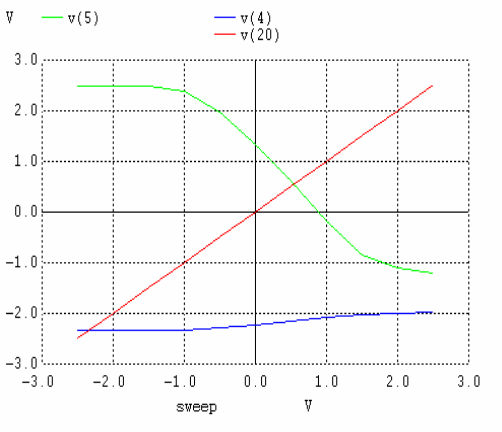

Fig.10: M1 drain v(5) , source v(4), and gate v(20) voltage according to the common mode input voltage.

V(5) is M1 drain voltage, V(4) is , M2 and M1 source voltage, and V(20) is M1,M2,M3,M4 gates voltage.

The AC simulation allows to represent the differential gain according to the input signal frequency.

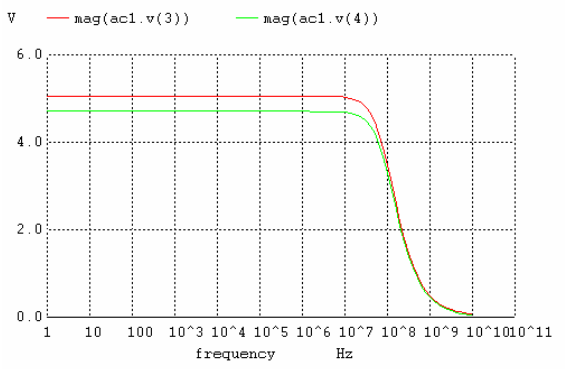

Fig.11 : differential gain according to the input signal frequency

The low frequency differential gain ,is defined by:

$$A_{VD}=\frac{V_{out+}-V_{out-}}{V_{in+}-V_{in-}} \qquad (10)$$

In differential mode V_{in+}=-V_{in-}, and V_{out+}=-V_{out-}

And:

$$A_{VD}=\frac{V_{out+}}{V_{in+}} \qquad (11)$$

analytically:

$$A_{VD} = \frac{g_{m1} + \frac{\left(\frac{W}{L}\right)_{M11}}{\left(\frac{W}{L}\right)_{M8}} \cdot \frac{g_{m4}.g_{m8}}{g_{DS4} + g_{m8} + g_{DS8}}}{g_{DS1} + g_{m8} + g_{DS9} + g_{DS11}} \quad (12)$$

The loads transistors assembled in diode make that the differential exit has low impedance. It results from it that the differential gain has a low value.
On figure 11 we represent the differential gain amplitude according to the input signal frequency, we Remark that the differential gain is low because the output nodes have low impedance. We can also observe that the band width is important

VI. Conclusion:

The Rail-to-Rail stage structure which we were interested allows to appreciate the performances of an input stage using two complementary differential pairs. The objectives laid down by this study are well atteinds, namely the running of the rail-rail differential stage with symetrical output whose voltages depend little on the common mode.

VII. References

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[2] J.F. Duque Carillo, R. Peres and J. M. Valverde, « Biasing circuit for high input ewing operational amplifiers », vol 30, N° 2 , feb 1995.

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