Intrinsic Small-Signal Equivalent Circuit of GaAs MESFET's

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Abstract : Finite Element Time Domain Method is used to determine the intrinsic elements of a broad-band small-signal equivalent circuit (SSEC) of FET's. The values of the differents elements are calculated from the Y parameters of the intrinsic MESFET, which are obtained from the Fourier analysis of the device transient reponse to voltage-step perturbations at the drain and gate electrodes. The success of this analysis depends crucially on the accuracy of the values calculated for the instantaneous currents at the electrodes during the transient. As application we have determined the SSEC for the case of a vertical drain and source contacts GaAs MESFET's.

I. INTRODUCTION

Usually, the SSEC of a FET's is designed by choosing a topology, so that each element provides a lumped approximation to some physical aspect of the device. A SSEC which is commonly accepted is formed of fifteen different frequency-independent elements: eight of them corresponding to the external parasitic effects and normally considered independent of the bias point, and the other seven describing the intrinsic behavior of the FET and dependent on the biasing conditions. In this paper we describe a theoretical procedure to calculate the intrinsic elements of the FET SSEC starting from the Y parameters obtained by using of a Finite Element Method (FEM) simulation. The FEM includes all the mechanisms relevant to the transport in small semiconductor devices (non-stationary effects, velocity overshoot, etc).

For a given operating point, the Y parameters are obtained from the Fourier analysis of the device transient response to voltage-step perturbations at the drain and gate electrodes. The validity of the intrinsic SSEC proposed can be verified by checking the frequency dependence of the calculated elements.

II. THEORETICAL ANALYSIS

In this technique, we employ the Fourier decomposition of the FET response to transient excitations. Let us suppose that over the stationary operating point we apply a voltage-step perturbation of amplitude ΔV_j at electrode j, and that $I_i(t)$ is the current response at electrode i. the complex Yij parameter will be given by the relation between the Fourier components of both signals, and can be shown to be[1]:

$$Re[Yij(\omega)] = \frac{I_i(\infty) - I_i(0)}{\Delta V_j} + \frac{\omega}{\Delta V_j} \int_0 [I_i(t) - I_i(\infty)] \sin \omega t \ dt$$

(1)

$$Im[Yij(\omega)] = \frac{\omega}{\Delta V_j} \int_0 [I_i(t) - I_i(\infty)] \cos \omega t \ dt$$

(2)

where $I_i(0)$ and $I_i(\infty)$ are the stationary currents at electrode i before and after the voltage perturbation respectively.

Figure 1 shows the small-signal equivalent circuit of the intrinsic FET, where Cds, Cgs and Cgd correspond to the drain-source, gate-source and gate-drain capacitances respectively. Ri is the resistance of the ohmic channel between the source and the gate. gm_0 represents the steady-state transconductance, and τ the delay time of the transistor. gds is the drain conductance.

For a given bias point, the elements of this intrinsic equivalent circuit can be obtained from the complex Y parameter corresponding to that point.
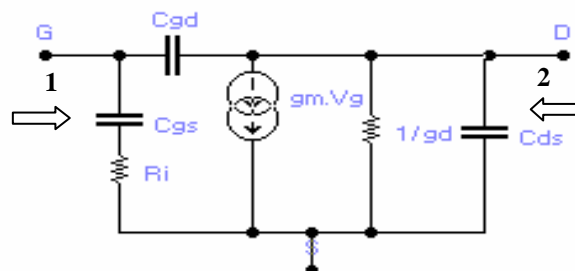
$$gm = gm_0 .\exp(-j\omega\tau)$$

Figure 1 : Small-signal equivalent circuit of the intrinsic FET

The *Yij* parameter will be given by a simple circuit analysis [2], [3]:

In the following, $i=1$ will stand for the gate and $i=2$ for the drain.

$$Y_{11}(\omega) = \frac{Ri.Cgs^2.\omega^2}{D} + j\omega\left(\frac{Cgs}{D} + Cgd\right) \quad (3)$$

$$Y_{12}(\omega) = -j.\omega.Cgd \quad (4)$$

$$Y_{21}(\omega) = \frac{gm_0.\exp(-j\omega\tau)}{1+j\omega.Ri.Cgs} - j.\omega.Cgd \quad (5)$$

$$Y_{22}(\omega) = gds + j\omega(Cgd + Cds) \quad (6)$$

with $\qquad D = 1 + \omega^2.Cgs^2.Ri^2$

From these expressions, and separating the *Y* parameters into their real and imaginary parts, the equivalent circuit elements can be found analytically:

$$Cgd = -\frac{Im[Y_{12}]}{\omega} \quad (7)$$

$$Cgs = \frac{Im[Y_{11}] - \omega.Cgd}{\omega}.\left(1 + \frac{(Re[Y_{11}])^2}{(Im[Y_{11}] - \omega.Cgd)^2}\right) \quad (8)$$

$$Ri = \frac{Re[Y_{11}]}{(Im[Y_{11}] - \omega.Cgd)^2 + (Re[Y_{11}])^2} \quad (9)$$

$$gm_0 = \sqrt{(Re[Y_{11}])^2 + (Im[Y_{21}] + \omega.Cgd)^2.(1+\omega^2.Cgs^2.Ri^2)} \quad (10)$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{-\omega.Cgd - Im[Y_{21}] - \omega.Cgs.Ri.Re[Y_{21}]}{gm}\right) \quad (11)$$

$$Cds = \frac{Im[Y_{22}] - \omega.Cgd}{\omega} \quad (12)$$

$$gds = Re[Y_{22}] \quad (13)$$

The program used in simulation contains the implementation of Poisson's equation and the current continuity equation in discrete form by the use of the finite element method [4]. A self consistent solution to the two equations is found by using a Scharfetter-Gummel approach [5], where Poisson's equation and current continuity equation are solved after each time step until the solution has converged. The classical semiconductor equations assume that the carrier velocities are an instantaneous function of the local electric field and that the mobility and diffusion coefficients are functions of electric field alone (some models take into account further temperature dependence).

The choice of a suitable diffusivity model poses some fundamental problems. As is well know, for fields below the threshold field, the diffusivity can be defined through a generalized Einstein relationship:

$$D(E) = \mu(E).\frac{K_b T_n}{q} \quad (14)$$

where K_b is the Boltzmann coefficient and T_n is the electron temperature assumed isotropic.

This relationship becomes invalid for $E>E_C$. In this case, the diffusivity may be modeled as an Einstein relation in lattice temperature *T* with one additional Gaussian term, to give [6]:

$$D(E) = \mu(E).\frac{K_b T}{q} + 800\exp\left[-\left(\frac{E-4000}{1650}\right)^2\right] \quad (15)$$

The diffusivity dependence on the electric field has been computed according to the relations (14) and (15). Figure 3 represents a comparison between these results and those obtained from Monte Carlo simulations of Pozela and Reklaitis [7].
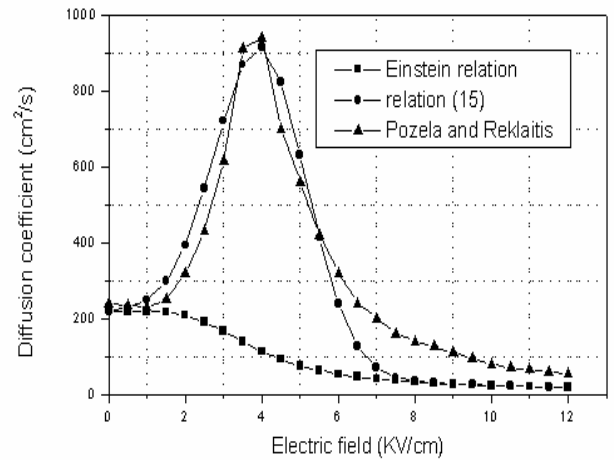

Figure 2: Several models of the diffusivity-electric field relation at room temperature

III. RESULTS AND DISCUSSION

The simulated results (MEF) of the current versus gate-voltage curves of the device (figure 3) compared with the meaured reults MEAS) [8] are shown in figure 4. A variable mesh spacing is used to optimize speed and accuracy of the solution (Figure 4). The mesh spacing criteria was based on the potential difference between the mesh nodes. The space steps are restrained to a maximum of a Debye length in the active channel and for numerical stability it has been found that an average step width of around 0,03 µm in the active channel is necessary for a doping level of $1.10^{16} cm^{-3}$.

In order to achieve a physically meaningful solution, the time step Δt is limited to less than the dielectric relaxation time and to avoid degrading the accuracy of the numerical solution, Δt is usually selected to lie in the range (10 to 25) fs.
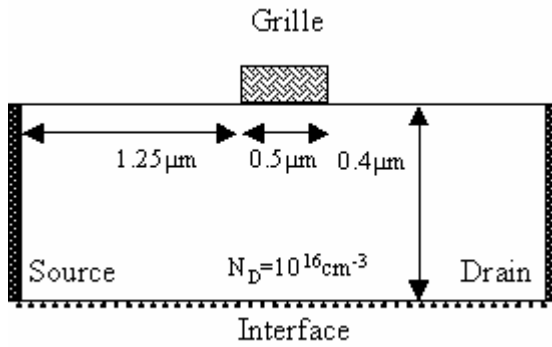

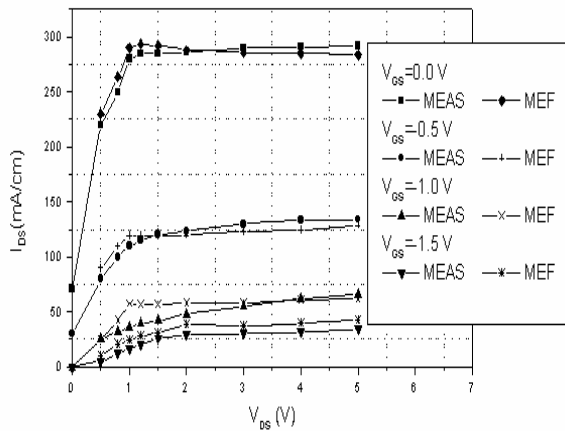**Figure 3:** Two-dimensional cross section of a 0.5µm MESFET geometry

Figure 4 : Comparison of the simulated characteristics I-V with Finite Element Method and measured [8]

Transient data

The device was also analyzed with regard to their transient behaviors. In order to determine the four Y parameters, two excitations are needed: one in the gate voltage and the other in the drain voltage. It must be stressed that the voltage-step amplitude must be sufficiently small, so as to avoid harmonic excitation in the device response, and large enough to get significant variations in the currents that dominate over numerical and physical noise. We have applied $\Delta V_1 = 0.125V$ for the case of the gate and $\Delta V_2 = 0.5V$ for the case of the drain.

Figure 5 illustrates the transient response of the gate and the drain currents at the bias point $V_{GS} = -1.0V$, $V_{DS} = 2.0V$.

A significant source current was found only during the first 1ps after the step was applied. This spike is proportional to the time derivative of the applied voltage perturbation and is pure displacement current. The correct evaluation of these current spikes is essential [1]. In our case this is assured by the value adopted for the time step (10fs) in the simulation, which is small enough to this purpose. The duration of the transient changes depending on the operating point.

The intrinsic *Y* parameters were obtained from the transients of figure 8 by means of (1) and (2).

The final step in this procedure is to apply (7)-(13) to the previous Y parameters in order to determine the values of the SSEC elements. The dependence on frequency of the intrinsic elements obtained in this way is shown in figure 6. Before averaging the parameters over frequency, we plot versus frequency the relative parameter, defined as an offset plus the parameter at frequency point divided by the average. With the exception of the transconductance which varies slightly according to the frequency and the channel resistance which starts to decrease from 32 GHz. It can be observed that all of them are frequency constant at least-up to 55 GHz. This means that the proposed SSEC describes correctly the AC behavior of the MESFET for this bias point, where the drain current is not very high and the accumulation of carriers between the gate and the drain is not important.

The value of cut-off frequency f_T can be calculated by dividing *gm* by ($Cgs + Cgd$).

We get $f_T = 15$. GHz.

CONCLUSION

A finite element method for the calculation of the FET SSEC has been described and applied to MESFET's. The method consists in the excitation of the different elements from the frequency dependent Y parameters of the intrinsic FET, obtained from the Fourier analysis of the device transient reponse to voltage perturbations at the terminals. finally, the finite element method, which uses a correcting factor to model the field-dependent diffusivity-to-mobility ratio, has been a powerful tool to check the validity of small-signal models.
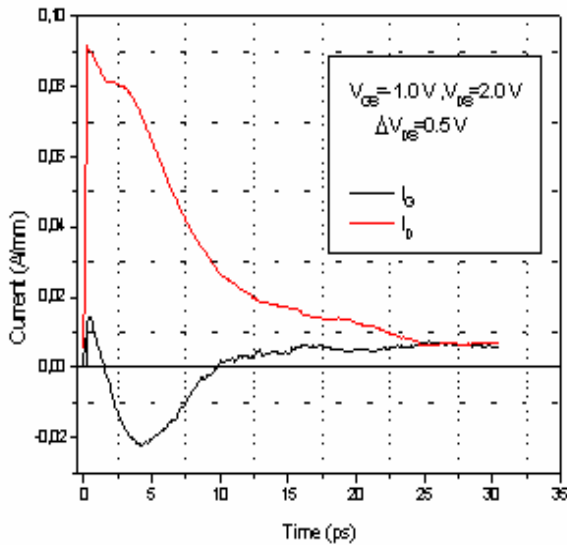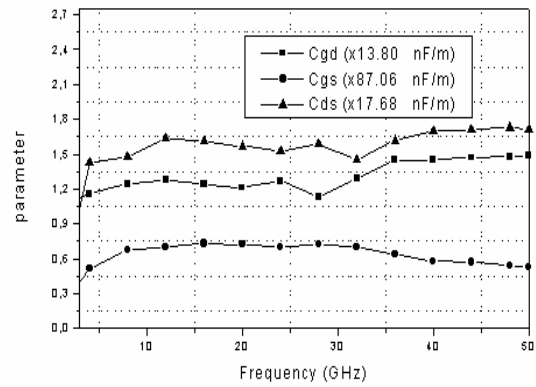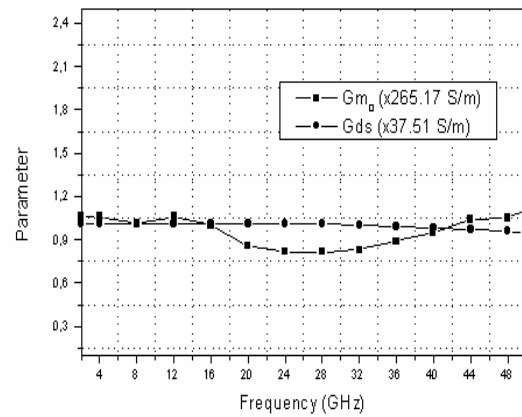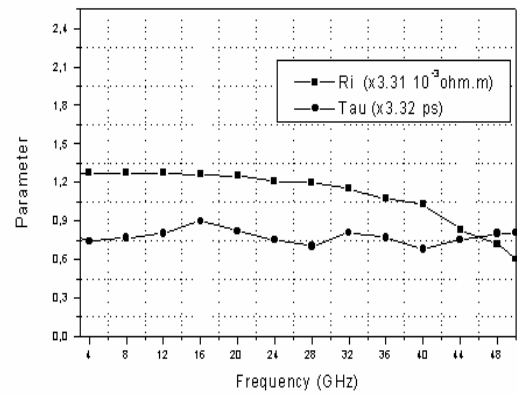

a)
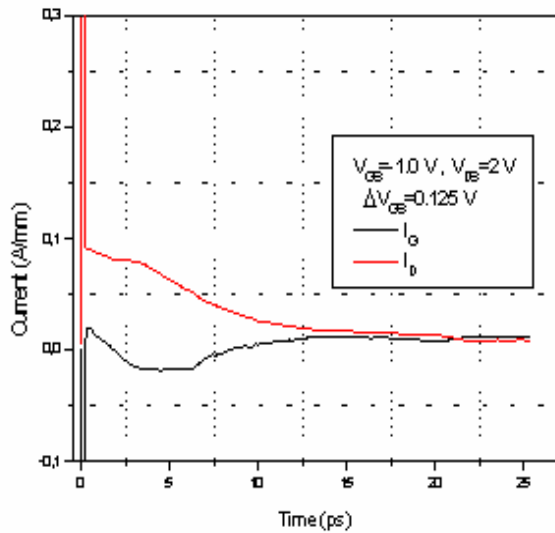
b)

Figure 5 : Transient reponse in the gate and drain currents of MESFET to a voltage step of amplitude and applied at t=0 over the stationary point corresponding to V_{GS}=-1.2V, V_{DS}=1.5V. (a) ΔV_{GS}=0.125V , (b) ΔV_{DS}=0.5V

a)

b)

c)

Figure 6 : Elements of the intrinsic small-signal equivalent circuit at the working point in saturation corresponding to V_{GS}=-1.V, V_{DS}=2.V. (a) capacitances, (b) conductances, (c) intrinsic resistance and delay time.

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